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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/787,326 | 02/26/2004 | Guenter Stenz | X-1478 US | 3972 |

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| EXAMINER | |
|---|---|
| SIEK, VUTHE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

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|---|---|
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/787,326 | STENZ ET AL. | |
| | Examiner | Art Unit | |
| | Vuthe Siek | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-12,14-22 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12,14-22 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/787,326 and RCE dated 3/9/07 with amendment dated 1/9/07. Claims 1-2, 4-12, 14-22 and 24-30 remain pending in the application, where claims 3, 13 and 23 are canceled.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-12, 14-22 and 24-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Hwang et al. (6,457,164 B1).

4. As to claims 1, 11 and 21, Hwang et al. teach a method for designing a programmable logic device (summary) comprising defining modules of a circuit design comprising components of a same type (implemented modules, SIMs; col. 5 lines 28-55; col. 5 lines 64-67; col. 6 lines 1-8; col. 7 lines 30-46); prior to annealing the circuit design, determining a set of static shapes for each module (a plurality of shapes for precomputed placements a given SIM; col. 5 lines 64-67; col. 6 lines 1-27; col. 7 lines 23-67; col. 8 lines 1-4; col. 10 lines 27-45); annealing the circuit design to determine a floorplan by, at least in part, for each module during a first iteration of annealing, selecting a shape from the set of static shapes associated with module and applying the selected shape to the module (col. 7 lines 23-67; col. 8 lines 1-4; for at least one module during at least one further iteration of annealing selecting a different shape from the set

of static shapes associated with the at least one module (plurality of pre-computed shapes for each module) and applying the different shape to the at least one module (col. 7 lines 23-67; col. 8 lines 1-35; col. 10 lines 27-45; col. 23 lines 56-67; col. 24 lines 1-56; Fig. 18-25 show examples), wherein each iteration of annealing the circuit design is evaluated according to evaluation of a cost function (col. 6, col. 7, lines 30-67; col. 10 lines 27-45; col. 24 lines 1-20).

5. As to claims 2, 12 and 22, Hwang et al. teach splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type (col. 5 lines 40-67, col. 6 lines 1-27).

6. As to claims 4, 14 and 24, Hwang et al. teach annealing comprising assigning modules and assigned shapes to locations on the programmable logic device (col. 6 lines 1-27; col. 7 lines 30-67; col. 8 lines 1-24; col. 24 lines 1-20).

7. As to claims 5, 15 and 25, Hwang et al. teach swapping locations of component of a same type that have associated grid sites, swapping two modules in a sequence pair, and switching the shapes of a module from one shape in the set of shapes associated with that module to another (col. 22). Note that swapping or changing placements between pair of modules are common practice in floorplanning of IC design layout (col. 27 lines 27-67).

8. As to claims 6, 16 and 26, annealing using bipartite matching of individual components is common practice in placement optimization, therefore it must be used during annealing as taught Hwang (col. 23 lines 40-67; col. 24 lines 1-20).

9. As to claims 7, 17 and 27, Hwang et al. teach identifying modules that share a timing critical path (share resources) and moving identified closer to one another (col. 25-26). Moving modules closer to each is common practice in layout IC design in order to minimizing interconnection.

10. As to claims 8, 18 and 28, Hwang et al. programmable logic is a Field Programmable Gate Array (FPGA, summary).

11. As to claims 9, 19 and 29, Hwang et al. each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed macro to be placed within that module (col. 25 lines 32-67; col. 26 lines 5-67). Note that a module or SIM and sub-modules or sub-SIMs or child SIM include width and height, a minimum width and height as well.

12. As to claims 10, 20 and 30, Hwang et al. teach generating a flat placement flow for the circuit design and comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan (col. 23 lines 40-67; col. 24 lines 1-67; col. 25 lines 1-67; col. 26 lines 1-21).

***Remarks***

13. Hwang et al. also teach creating a plurality of shapes for each module for placement optimization using simulated annealing software tool based cost function (see above rejection). Examiner respectively submits that the amended claims present are not allowable.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

Vuthe Siek

**VUTHE SIEK**
**PRIMARY EXAMINER**